Notice of Allowability	Application No.	Applicant(s)	
	10/791,292	ABUGHAZALEH ET AL.	
	Examiner	Art Unit	
	John B. Vigushin	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Application filed 03 March 2004*.

2. ☒ The allowed claim(s) is/are *1-25*.

3. ☒ The drawings filed on *03 March 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 1104//01 Nov 2004
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Allowable Subject Matter

1. Claims 1-25 have been allowed.

2. The following is an examiner's statement of reasons for allowance:

In Claims 1-16, patentability resides in **the combination of** *a communication circuit disposed on at least a first layer of the plurality of layers and electrically coupled between an insulation displacement connector (IDC) at a PD/User end and an RJ45 connector at a telecommunication equipment end*, **and** *at least one of a removable modular or fixed electronic component electrically coupled with the communication circuit, the component comprised of at least one active circuit disposed on at least a second layer of the plurality of layers*, in further combination with the other limitations of base Claim 1.

As to Claims 17-25, patentability resides in **the combination of** *disposing upon at least a first layer of the plurality of layers a communication circuit, the communication circuit electrically coupled between an insulation displacement connector (IDC) at a PD/User end and an RJ45 connector at a telecommunication end*, **and** *disposing upon at least a second layer of the plurality of layers at least one of a removable modular and fixed electronic component electrically coupled with the communication circuit, the component comprised of at least one active circuit*, in further combination with the other limitations of base Claim 17.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Phommachanh (US 6,089,923) discloses all the limitations of originally filed base Claims 1 and 17 (multilayer patch panel 40 in Fig. 5; layers 1-4 in Figs. 6-9, respectively, a communication circuit on each layer containing signal carrying traces and *compensation circuitry that includes conductive lines 52 disposed in parallel to form capacitors 52C*; *RJ45 connectors connected to one side of board 40 and IDC connectors mounted on the opposite side, the RJ45 connectors and IDC connectors interconnected through the compensation circuitry*; col.4: 50-63; col.5: 58-col.7: 17; Category 6 crosstalk suppression standards are met: col.2: 17-30 and col.8: 23-29) with the exception of *at least one of a removable modular or fixed electronic component comprised of at least one active circuit disposed on at least a second layer of the plurality of layers of patch panel circuit board 40.*

b) Aekins (US 5,931,703) discloses all the limitations of originally filed base Claims 1 and 17 (including a three layer patch panel circuit board 20 in Fig. 2 labeled as layers 66, 67 and 68--see Figs. 3-5; col.4: 26-31; col.5: 54-59--wherein a communication circuit, containing signal carrying traces and compensation circuitry, is disposed on at least a first layer of board 20--see col.5: 26-48--and wherein middle layer

67 is a compensation separation mechanism disposed between the first and second layers 66 and 68: see col.6: 14-28; Category 5 crosstalk suppression standards are met: col.3: 48-58) with the exception of *at least one of a removable modular or fixed electronic component comprised of at least one active circuit disposed on at least a second layer of the plurality of layers of patch panel circuit board 40.*

c) Aekins (US 6,057,743) discloses all the limitations of originally filed base Claims 1 and 17 including RJ45 and IDC connectors mounted on a multilayer patch panel circuit board 20 (Fig. 1; col.2: 40-46; col.4: 3-7) and a communication circuit, containing signal carrying traces and compensation circuitry on at least a first layer of the plurality of layers in patch panel board 20 (Figs. 2-5; col.5: 27-49), *the compensation circuitry including capacitive and inductive structures formed from the conductive traces of the circuitry* (col.5: 55-64; col.6: 16-29); Category 4, 5, 5e and 6 crosstalk suppression standards are met (col.2: 47-53; col.6: 48-col.7: 11). Aekins does not teach *at least one of a removable modular or fixed electronic component comprised of at least one active circuit disposed on at least a second layer of the plurality of layers of patch panel circuit board 20.*

d) Bullivant et al. (US 5,944,535) discloses all the limitations of originally filed base Claims 1 and 17 including the compensation layer 67 on a patch panel circuit board 28 having three circuit layers 66, 67 and 68, *similar to the structure of Aekins (US 6,057,743)*, discussed above, and meeting Category 5 crosstalk suppression standards (col.5: 39-45).

e) Aekins (US 6,533,618 B1) discloses all the limitations of originally filed base Claims 1 and 17 including the RJ45 and IDC connectors mounted on patch panel circuit board 4 (Fig. 3; col.6: 39-42) and a communication circuit containing signal carrying traces and compensation circuitry (comprising positive and negative *reactance circuitry*; col.10: 26-36) on the top and bottom surfaces of the patch panel board 4 (Figs. 4 and 5; col.7: 36-45; col.8: 13-64) but does not teach *a compensating separation mechanism comprised of a third layer disposed between the first (top) and second (bottom) layers of patch panel board 4* and does not teach *at least one of a removable modular or fixed electronic component comprised of at least one active circuit disposed on at least a second layer of the plurality of layers of patch panel circuit board 4.*

f) Chen (US 6,483,715 B1) discloses all the limitations of originally filed base Claims 1 and 17 (RJ45 and IDC connectors and a patch panel circuit board 20 with a communication circuit disposed on both sides of board 20 containing signal carrying traces and compensation circuitry on the two sides of the circuit board 20, the compensation circuitry formed as part of the interconnection circuitry and including capacitors 41, 42 and inductors 51a,b 52a,b formed integrally with the conductive lines of the interconnection circuitry; Figs. 2A,B and 3A,B; col.2: 66-col.3: 2; col.3: 53-col.4: 63; category 6 crosstalk suppression standards are met: col.2: 11-13) with the exception of *a compensation separation mechanism comprised of at least a third layer disposed between the first and second layers* and *at least one of a removable modular or fixed electronic component comprised of at least one active circuit disposed on at least a second layer of the plurality of layers of patch panel circuit board 20.*

g) Hipp et al. (US 6,411,506 B1) discloses a passive midplane 34 with DIMMs (col.9: 27-34; col.10: 28-38) and CPUs (col.7: 63-col.8: 5) connected to one side and network interface cards connected to the opposite side (Figs. 1 and 4-7; col.3: 44-col.4: 27) using RJ45 connectors (col.12: 13-19); Category 5 communication cable 44 is used (col.12: 9-13); industry standard rack of 42 U is employed (col.8: 57-64); passive midplane 34 auto-senses CPU cards and available connector slots to allow automatic configuration of networks via remote management system 70 (col. 15: 43-50).

h) Berding (US 5,930,119) discloses a passive backplane having compensation circuitry that reduces LC product inherent in the conductive traces, thereby reducing signal propagation delay (Figs. 2-5; col.5: 31-61; col.6: 33-39).

i) Berding (US 6,512,396) discloses a backplane with compensation circuitry (Fig. 5) and *active components*--i.e., *boost circuits 200 and 204* (Figs. 5 and 6)--for reducing signal rise and fall times (col.4: 55-col.5: 28) and passive components--i.e., damping resistors 903 (Fig. 5)--for line termination and elimination of signal reflection (col.6: 18-50). Berding does not teach *a communication circuit disposed on at least a first layer of the plurality of layers and electrically coupled between an insulation displacement connector (IDC) at a PD/User end and an RJ45 connector at a telecommunication equipment end*; rather, Berding teaches only a backplane with card connector slots and configured in accordance with a VME or PCI standard (Fig. 5; col.3: 10-14) for receiving modular circuits in a computer (col.1: 14-19).

j) Balakrishnan (US 4,697,858) discloses an active backplane having removable daughterboards 108 on one side and transceiver chips 106 on the opposite side, the

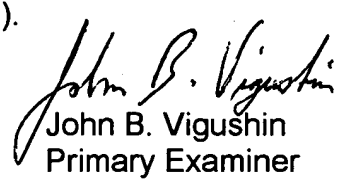
placement of the transceivers 106 on the backplane saving space on the daughterboards and improving the electrical performance of the backplane (col.6: 37-41); the backplane including ground planes 112 and 114 for shielding bus lines 110 and reducing crosstalk (col.4: 28-33; col.5: 45-51).

k) Thompson et al. (US 5,748,451) discloses, in Figs. 1 and 3, an active backplane 12 (col.1: 11-25) provided with a stiffener (substrates 14 and 16), the stiffener substrate 16 having connectors 22--for receiving removable voltage regulator cards or power supply cables in order to provide power or other signals to active backplane 12--and further having decoupling capacitors 26 mounted thereon for power and/or signal line noise suppression (col.3: 10-30). Active backplane 12 has cards 32 mounted directly thereto (Fig. 3; col.3: 65-col.4: 29).

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
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